1.	Name of Course				Digital Systems					
2.	Course Code				CCPS1573					
3.	Name(s) of academic staff									
4.	Rationale for the inclusion of the course/module in the programme				Faculty This module provides foundation knowledge which is necessary for the understanding of other modules such as CCP0102 Computer Architecture. It is therefore imperative that student of computer related fields are offered the opportunity to gain experience of design and implementation of simple circuits and understand the principle of computer hardware.					
5.	Semester and Year offere	d			1/1					
6.			Face to	Face	Total Guided and Independent Learning					
	L = Lecture T = Tutorial P = Practical O= Others	L 28	T	P 28	0	Independent = 84 Total =140				
7.	Credit Value				3					
8.	Prerequisite (if any)				None					
9.	Objectives: To familiarise the student with binary and hexadecimal number system. To familiarise the student with the fundamental operation of digital circuit elements. To introduce the fundamental concepts of logic design of digital circuits. To introduce digital circuit design at the combinatorial and simple sequential level.									
10.	Learning outcomes:									
	 After completing this subject, it is expected that students will able to: Explain the fundamentals of digital circuit logic elements, various logical operations and design of logic circuits. Explain the functionalities of basic building blocks of a microcomputer. Utilise laboratory equipment and their documented laboratory work to perform exercises in a manner consistent with good computing practice. Undertake relevant analysis of simple electronic circuits. 									
11.	Familiarise withFamiliarise with	binary basic	/ and h analog	nexadeo gue and	cimal nu I digital	gn of digital circuits. Imber system. electronics and develop circuit analysis skills. Ving system problems				

		hing-learning and assessment strategy riety of teaching and learning strategies are used throughout the course, including:											
	•	Classroom lessons: Lectures and Power Point presentations											
	•	Laboratory sessions: Practice exercises											
	•	brainstorming;											
	•	student-Lecturer discussion											
	•	collaborative and co-operative learning;											
	•	Independent study.											
	Assessm	ent strateg	gies incluc	de the follo	wing:								
	•	ment strategies include the following: Ongoing quizzes											
	•	Midtern	n tests										
	•	Perform	ance Asse	essment (pr	roject, Assigne	ed exercises)							
	•	Lecturer	Observat	tion									
13.	Synops												
				cpose stude	nt to the field	d of Digital tec	nnology elem	ents such as	Logi	c elem	nents,	Count	ers
		sters and e	tc.										
14.		Delivery:											
	•					oint presentati	ons						
45	•			ns: Practice	e exercises								
15.		ent Metho			ased on the f	following:							
	THE asse	331116111 101	tilis coul	se will be t	aseu on the i	ollowing.		Coursew	ork				50%
		Quizzes			15%			Coursew	OIK				30%
		assignm			15%								
	•	•		am	20%								
		Mid-Semester Exam 20% Final Exam 50%								50%			
													100%
16.						Ma	pping of the c	ourse/mod	ule to	o the F	Progra	amme	Aims
16.	A1		.2	A3	A4	A5	A6	A7	ule to	A8		P	۱9
	A1 3		1	A3 1	1	A5 1	A6 1	A7		A8 1	_	F	N9 0
16.	3		1	1	1 Марј	A5 1 ping of the co	A6 1 urse/module	A7 1 to the Prog	ramn	A8 1 ne Lea	ırning	Outco	0 omes
	3 LO1	LO2	LO3	1 LO4	1 Mapp LO5	A5 1 ping of the co	A6 1 urse/module	A7 1 to the Prog	ramn LO:	A8 1 ne Lea 10	rning	Outco	0 0 0 0 0 0 0 1 0 1 1 1 1
17.	3		1	1 LO4 0	Mapp LO5	A5 1 ping of the co LO6 LO 0 1	A6 1 urse/module LO8 2	A7 1 to the Prog	ramn	A8 1 ne Lea 10	ırning	Outco	0 omes
	3 LO1	LO2	LO3	1 LO4 0	Mapp LO5	A5 1 ping of the co	A6 1 urse/module LO8 2	A7 1 to the Prog	ramn LO:	A8 1 ne Lea 10	rning	Outco	0 0 0 0 0 0 0 1 0 1 1 1 1
17.	3 LO1	LO2	LO3	1 LO4 0	Mapp LO5	A5 1 ping of the co LO6 LO 0 1	A6 1 urse/module LO8 2	A7 1 to the Prog	ramn LO:	A8 1 ne Lea 10	LO1:	Outco	0 0 0 0 0 0 0 1 0 1 1 1 1
17.	3 LO1	LO2	LO3	1 LO4 0	1 Mapp	A5 1 ping of the co LO6 0 1 course/modu	A6 1 urse/module LO8 2	A7 1 to the Prog	ramn LO:	A8 1 ne Lea 10	LO1:	Outco	0 omes LO12 0
17.	3 LO1	LO2	LO3	1 LO4 0	Mapp LO5	A5 1 ping of the co LO6 0 1 course/modu	A6 1 urse/module LO8 2	A7 1 to the Prog	ramn LO:	A8 1 ne Lea 10	LO1:	Outco	0 omes LO12 0
17.	3 LO1	LO2	LO3	1 LO4 0	1 Mapp	A5 1 ping of the co LO6 0 1 course/modu	A6 1 urse/module LO8 2	A7 1 to the Prog	ramn LO:	A8 1 ne Lea 10	LO1:	Outco	0 0 0 0 0 0 0 1 0 1 1 1 1
17.	LO1 3	LO2	LO3	1 LO4 0	1 Mapp	A5 1 ping of the co LO6 0 1 course/modu	A6 1 urse/module LO8 2	A7 1 to the Prog	ramn LO:	A8 1 ne Lea 10	LO1:	Outco	0 omes LO12 0
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17.	LO1 3	LO2	LO3 0	LO4 0 Content o	1 Mapp LO5 1 Dutline of the	A5 1 ping of the co LO6 LO 0 1 course/modu ails	A6 1 urse/module LO8 2 le and the SL	A7 1 to the Prog LO9 0 T per topic Introduc	ramn LO: 1	A8 1 ne Lea 10	LO1:	Outco	0 omes LO12 0
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17.	10pic 1	LO2 2	LO3 O Digita	LO4 0 Content of	LO5 1 Dutline of the Deta	A5 1 ping of the co LO6 LO 0 1 course/modu ails	A6 1 urse/module LO8 2 le and the SL as, Binary/Oct s: BCD, Excess	A7 1 to the Prog LO9 0 Fer topic Introduc al/Hex Nun 5-3, Gray, A Logic Elem circuit out	ramn LO2 1 1 strict on the control of the control o	A8 1 ne Lea 10	LO1:	Outco L I	N9 0 omes LO12 0
17.	LO1 3	LO2 2	LO3 O Digita	LO4 0 Content of	LO5 1 Dutline of the Deta	A5 1 ping of the co LO6 LO 0 1 course/modu ails lumber Syster ic. Other Code	A6 1 urse/module LO8 2 le and the SL as, Binary/Oct s: BCD, Excess	A7 1 to the Prog LO9 0 Fer topic Introduc al/Hex Nun 5-3, Gray, A Logic Elem circuit out	ramn LO2 1 ttion hber SCII. ents out , and	A8 1 ne Lea 10 L	DOI:	Outco L I	0 omes LO12 0 ret of LO12 10

	Topic 3	Combination Logic Circuit Sum-of-Product&Product-of-Sum, Simplification of Logic Circuit .Designing Combinational Logic. K-Map, Basic characteristics of Digital ICS. XOR and XNOR circuits, and Parity generator.	4	4	12	20		
	Topic 4	Sequential Logic. Delays & Latches, Clock signal, JK & Flip- flops.D flip –flops, Timing & State, Asynchronous inputs, Master/slave flip-flop, Flip-flop synchronisation and application. Monostable and astable multivibrators.	3	3	9	15		
	Topic 5	Arithmetic Circuits. Signed numbers.2's complement, Addition & subtraction, Multiplications and Division, BCD Addition, Half & Full Adder, Parallel/Aerial Adder and Carry propation.	3	3	9	15		
	Topic 6	MSI Logic circuits Decoder/Encoder, 7 – Segment drivers, Multiplexer & Demultiplexer, Code Converter & Comparators and Tristate register.	3	3	9	15		
	Topic 7	Counters and Register Synchronous/Asynchronous counters. Up/down counters, Design counters, Shift register Parallel & series load). Counter / Shift register ICs	3	3	9	15		
	Topic 8	and Counter/Shift applications IC logic families TTL/CMOS/ECL Characteristics, Loading & Fan-out, Open Collectors & Open drain and Tristate TTL	2	2	6	10		
	Topic 9	Interfacing with analogue devices DAC &ADC, Converter circuits and Digital-ramp ADC.	2	2	6	10		
	Topic 10	Memory Devices Memory Architecture, Memory Operations, CPU-memory Connection, ROM/RAM/EPROM And Read/Write Cycle.	2	2	6	10		
		Total	28	28	84	140		
	Laboratory	Laboratory Details Exercises based on topics covered in each lecture. Experimental work must Introduction to basic tools (breadboard, oscilloscope, IC tester, etc.) Build simple circuits using basic gates design & implement combinational logic circuits Implement flip-flops Design & implement couters and shiftregisters Design & implement Arithmetic circuits & Arithmetic ICs Design & implement decoder/encoders Simple projects	includ	de the	e follo	owing		
19.		eferences supporting the course: 5 L. Floyd, "Digital Fundamentals" 10th Edition, Pearson Education International, 2008.						
	Additional references supporting the course: 1. M.Moris Mano and Michael D. Ciletti, "Digital Design", 4 th Edition, 2007, Prentice hall. 2. Ronald J. Tocci, Neal S.Wldmer, and Gregory L.Moss, "Digital Systems: Principles and Application", 10th Edition, Pearson education International, 2007							

Bachelor of Computer Science (Hons)

20.	Other additional information
	All materials will be available to the students online.

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