<table>
<tr><td>1.</td><td colspan="5">Name of Course</td><td>Digital Logic Design</td></tr>
<tr><td>2.</td><td colspan="5">Course Code</td><td>JDLD1033</td></tr>
<tr><td></td><td colspan="6">JDLD = the first alphabet identify the faculty within which the subject is offered., JDLD = the remaining three alphabets identify the course that offers the subject, 1033 = the first digit identify level of study; in this case undergraduate level, 1033 = the second and third digits identify subject identity and 1033 = the fourth digit identify credit value or credit hours</td></tr>
<tr><td>3.</td><td colspan="5">Name(s) of academic staff</td><td>To be Assigned</td></tr>
<tr><td>4.</td><td colspan="5">Rationale for the inclusion of the course/module in the programme</td><td>Knowledge of digital logic design is essential in electrical and electronics engineering. Moreover, acquiring knowledge in logic circuit enable engineer to design digital system.</td></tr>
<tr><td>5.</td><td colspan="5">Semester and Year offered</td><td>Year 1, Semester 2</td></tr>
<tr><td rowspan="3">6.</td><td colspan="2" rowspan="2">Total Student Learning Time (SLT)</td><td colspan="4">Face to Face</td><td rowspan="2">Total Guided and Independent Learning</td></tr>
<tr><td rowspan="2">L = Lecture T = Tutorial
P = Practical
IS= Independent Study</td><td>L</td><td>T</td><td>P</td><td>IS</td><td rowspan="2">Total Guided and Independent Learning = 120</td></tr>
<tr><td>42</td><td>7</td><td>6</td><td>65</td></tr>
<tr><td>7.</td><td colspan="5">Credit Value</td><td>3.0</td></tr>
<tr><td></td><td colspan="6">Lecture: 3 hours per week x 14 weeks
Tutorial 1 hour per week x 7 weeks
Practical: 2 hours x 3 weeks</td></tr>
<tr><td>8.</td><td colspan="5">Prerequisite (if any)</td><td>None</td></tr>
<tr><td>9.</td><td colspan="6">Course Objectives
1. To equip the students with the knowledge of the digital logic design.

Course Learning Outcomes (CLO)
At the end of the semester students should be able to:

CLO1: Describe the differences between analog and digital systems, and their respective advantages and disadvantages;
CLO2: Analyze and design combinational and sequential logic circuit;
CLO3: Apply algebraic methods based on Boolean algebra and truth table to.</td></tr>
<tr><td>10.</td><td colspan="6">Transferable Skills:
This course is expected the development of the following transferable skills:
▪ An ability to manage time and task
▪ An ability to learn both independently and co—operatively;
▪ An ability to take responsibility and carry out laboratory test;
▪ An ability to take initiative and lead other;
▪ An ability to use software where relevant to the subject.</td></tr>
<tr><td>11.</td><td colspan="6">Teaching-learning and assessment strategy

A variety of learning strategies are used throughout the course, including the following
• Classroom Lesson; Lecturer and power point presentation
• Tutorial session
• Student- lecturer Discussion
• Collaborative and co-operative learn;
• Independent study.</td></tr>
</table>

	Assessment:		
	Course works		**40%**
	Assignment	5%	
	Tutorial	5%	
	Quizzes	5%	
	Laboratory works	10%	
	Test	15%	
	Final Examination		**60%**
	Total		**100%**
12.	**Synopsis:** This course is very important course in the field of digital logic design. The objective of course is to provide a basic understanding of the basics of digital logic circuits and their applications in digital system.		
13.	**Mode of Delivery:** Lectures; Tutorials; Laboratory works		

14.	**Assessment Methods and Types:** **Performance Criteria :**						
	CLO-PLO	**Assessment Tool**	**1**	**2**	**3**	**4**	**5**
	Marks		**0-39**	**40-49**	**50-59**	**60-74**	**75-100**
	Grade		**(F)**	**(D,D+)**	**(C-,C,C+)**	**(B-,B,B+)**	**(A-,A,A+)**
	CLO1: To Describe the differences between analog and digital systems, and their respective advantages and disadvantages.	**Assignment** **Tutorials** **Lab works** **Quizzes** **Test** **Examination**	**Fail To:** - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Poor To**: - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Satisfactory To**: - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Good To**: - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Excellent To:** - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test
	CLO2: To Analyze and design combinational and sequential logic circuit;	**Assignment** **Tutorials** **Lab works** **Quizzes** **Test** **Examination**	**Fail To:** - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Poor To**: - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Satisfactory To**: - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Good To:** - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Excellent To:** - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test
	CLO3: Apply algebraic methods based on Boolean algebra and truth table.	**Assignment** **Tutorials** **Lab works** **Quizzes** **Test** **Examination**	**Fail To:** - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Poor To**: - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Satisfactory To**: - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Good To**: - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Excellent To:** - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test

15. **Mapping of the Programme Objectives to the Programme Learning Outcomes**

Programme Learning Outcomes (PLO) / Programme Objectives (PO)	**PLO1:** Ability to acquire and apply knowledge of science and engineering fundamentals.	**PLO2:** Acquired in-depth technical competence in digital logic design engineering discipline.	**PLO3:** Ability to undertake problem identification, formulation and solution;	**PLO4:** Ability to utilise systems approach to design and evaluate operational performance.	**PLO5:** Understanding of the principles of design for sustainable development;	**PLO6:** Understanding of professional and ethical responsibilities and commitment to them.	**PLO7:** Ability to communicate effectively, not only with engineers but also with the community at large.	**PLO8:** Ability to function effectively as an individual and in a group with the capacity to be a leader or manager;	**PLO9:** Understanding of the social, cultural, global and environmental responsibilities of a professional engineer	**PLO10:** Recognising the need to undertake lifelong learning, and possessing/acquiring the capacity to do so	**PLO11:** Ability become entrepreneur
PO1: To produce graduates with excellent knowledge and competency in Electrical and Electronic Engineering;	✓			✓			✓				
PO2: To produce graduates with professional, generic attributes to meet the present and future global demands;							✓				
PO3: To produce graduates with Islamic humanistic values and reinvention skills to meet the requirement of a dynamic environment. These skills include Civil Intelligence, Moral Intelligence, Self-Reliance and Communication Skills.							✓				

16. **Mapping of the course Learning Outcome to the Programme Outcome**

Programme Learning Outcomes (PLO) / Course Learning Outcome (CLO)	**PLO1:** Ability to acquire and apply knowledge of science and engineering fundamentals.	**PLO2:** Acquired in-depth technical competence in digital logic design engineering discipline.	**PLO3:** Ability to undertake problem identification, formulation and solution;	**PLO4:** Ability to utilise systems approach to design and evaluate operational performance.	**PLO5:** Understanding of the principles of design for sustainable development;	**PLO6:** Understanding of professional and ethical responsibilities and commitment to them.	**PLO7:** Ability to communicate effectively, not only with engineers but also with the community at large.	**PLO8:** Ability to function effectively as an individual and in a group with the capacity to be a leader or manager;	**PLO9:** Understanding of the social, cultural, global and environmental responsibilities of a professional engineer	**PLO10:** Recognising the need to undertake lifelong learning, and possessing/acquiring the capacity to do so	**PLO11:** Ability become entrepreneur
CLO1: Describe the differences between analog and digital systems, and their respective advantages and disadvantages.	✓			✓			✓				
CLO2: To Analyze and design combinational and sequential logic circuit.	✓			✓			✓				
CLO3: To apply algebraic methods based on Boolean algebra and truth table;	✓			✓			✓				

17.	Content outline of the course/module and the SLT per topic						
	Details		SLT (Hour)				
			L	T	P	IS	Total
	Topic 1	**Introduction** • Numerical Representation, • Digital and Analog Systems, • Digital Number Systems, • Representing Binary Quantities, • Digital Circuits/Logic Circuits, • Parallel and Serial Transmission, • Memory, • Digital Computers.	3	-	-	8	**11**
	Topic2	**Number Systems and Codes** • Binary-to-Decimal Conversions, • Decimal-to-Binary Conversions, • Hexadecimal Number System, • BCD Code, • The Gray Code, • Alphanumeric Codes	6	1	-	10	**17**
	Topic3	**Describing Logic Circuits** • Boolean Constants and Variables, • Truth Tables, • OR Operation with OR Gates, • AND Operation with AND Gates, • NOT Operation • Describing Logic Circuits Algebraically, • Evaluating Logic-Circuit Outputs, • Implementing Circuits from Boolean Expressions, • NOR Gates and NAND Gates, Boolean Theorems, • DeMorgan Theorems, • Universality of NAND Gates and NOR Gates • Alternate Logic-Gate Representations, • Which Gate Representation to Use, I • EEE/ANSI Standard Logic Symbols, • Description Languages Versus Programming Languages, • Implementing Logic Circuits with PLDs, HDL Format and Syntax	9	1	-	10	**20**

	Topic 4	**Combinational Logic Circuits** • Sum-of-Products Form, • Simplifying Logic Circuits, • Algebraic Simplification • Designing Combinational Logic Circuits, • Karnaugh Map Method, • Exclusive-OR and Exclusive-NOR Circuits, • Parity Generator and Checker, • Enable/Disable Circuits, • Basic Characteristics of Digital ICs, • Programmable Logic Devices	6	1	-	10	**17**
	Topic 5	**Sequential Logic Circuits** • NAND Gate Latch, • NOR Gate Latch, • Digital Pulses, • Clock Signals and Clocked Flip-Flops, • Clocked S-R Flip-Flop, Clocked J-K Flip-Flop • Clocked D Flip-Flop, • D Latch (Transparent Latch), • Asynchronous Inputs • IEEE/ANSI Symbols, • Flip-Flop Timing Considerations, • Potential Timing Problem in FF Circuits, • Flip-Flop Applications, Flip-Flop Synchronization • Detecting an Input Sequence, • Data Storage and Transfer, • Serial Data Transfer: • Shift Registers, • Frequency Division and Counting, • Schmitt-Trigger Devices, • One-Shot (Monostable Multivibrator), • Clock Generator Circuits	9	2	-	12	**23**

	Topic6	**Modular Combinational Logic** • Modular Design. Decoders. • Decoder Circuit Structures. • Implementing Logic Functions Using Decoder. • Encoder Circuit Structures. • Multiplexers/Data. • Selectors. • Multiplexer Circuit Structures. • Applications of Multiplexers. • Demultiplexers/Data Distributors. • Binary Arithmetic Elements. • Binary Adder Circuits. • Binary Subtraction Circuits. • Arithmetic Overflow Detection. Comparators. **Design Example**: • A Computer Arithmetic Logic Unit. **Computer-ai Counters and Registers** • Asynchronous (Ripple) Counters, • Propagation Delay in Ripple Counters, • Synchronous (Parallel) Counters, • Counters with MOD Numbers < 2N, • Synchronous Down and Up/Down Counters • Synchronous Counter Design, State Machines. • Ded Design of Modular Systems	9	2	-	15	**26**
	Practical	1. Combinational Logic Circuits And Their Applications 2. Sequential logic circuit And Their Applications 3. Counter design.	-	-	6	-	**6**
	Total SLT (Hour)		**42**	**7**	**6**	**65**	**120**
18.	**Main references supporting the course** 1. Tocci, R.J., "Digital Systems: Principles and Applications", 9th Ed, Prentice Hall 2006.						
	Additional references supporting the course 1. Alan B. Marcovitz, "Introduction to Logic Design", 3nd ed., McGraw-Hill, 2007 2. Ronald J. Tocci, Neal S. Widmer and Gregory L. Moss, "Digital Systems - Principles and Applications", 11th ed., Prentice-Hall, 2006 3. S. Brown and Z. Vranesic, "Fundamentals of Digital Logic with VHDL Design", 3rd ed., McGraw-Hill, 2007.						
19.	**Other additional information** All materials will be available to the students in the library.						