<table>
<tr><td>1.</td><td colspan="5">Name of Course</td><td>Digital VLSI System Design</td></tr>
<tr><td>2.</td><td colspan="5">Course Code</td><td>JDSD1133</td></tr>
<tr><td></td><td colspan="6">JDSD = the first alphabet identify the faculty within which the subject is offered., JDSD = the remaining three alphabet identify the course that offers the subject, 1133 = the first digit identify level of study; in this case undergraduate level, 1133 = the second and third digits identify subject identity and 1133 = the fourth digit identify credit value or credit hours</td></tr>
<tr><td>3.</td><td colspan="5">Name(s) of academic staff</td><td>To be Assigned</td></tr>
<tr><td>4.</td><td colspan="5">Rationale for the inclusion of the course/module in the programme</td><td>Knowledge of integrated circuit is essential in electronics engineering. Moreover, acquiring knowledge in semiconductor materials provide students with advanced knowledge in digital design techniques and methodologies.</td></tr>
<tr><td>5.</td><td colspan="5">Semester and Year offered</td><td>Year 3, Semester 1</td></tr>
<tr><td rowspan="3">6.</td><td colspan="2">Total Student Learning Time (SLT)</td><td colspan="4">Face to Face</td><td>Total Guided and Independent Learning</td></tr>
<tr><td colspan="2" rowspan="2">L = Lecture T = Tutorial
P = Practical
IS= Independent Study</td><td>L</td><td>T</td><td>P</td><td>IS</td><td rowspan="2">Total Guided and Independent Learning = 120</td></tr>
<tr><td>42</td><td>7</td><td>6</td><td>65</td></tr>
<tr><td>7.</td><td colspan="5">Credit Value</td><td>3.0</td></tr>
<tr><td></td><td colspan="6">Lecture: 3 hours per week x 14 weeks
Tutorial: 1 hour per week x 7 weeks
Practical: 2 hours x 3 weeks</td></tr>
<tr><td>8.</td><td colspan="5">Prerequisite (if any)</td><td>JDLD1033:Digital Logic Design</td></tr>
<tr><td>9.</td><td colspan="6">Course Objectives
1. To introduce VLSI;
2. To equip the students with the knowledge of digital design techniques and methodologies.

Course Learning Outcomes (CLO)
At the end of the semester students should be able to:

CLO1: To introduce the IC design techniques;
CLO2: To use engineering principles in hardware and software aspects of digital design;
CLO3: To design, test and analyze the VLSI digital system’s on FPGA platform.</td></tr>
<tr><td>10.</td><td colspan="6">Transferable Skills:
This course is expected the development of the following transferable skills:
▪ An ability to manage time and task
▪ An ability to learn both independently and co—operatively;
▪ An ability to take responsibility and carry out laboratory test;
▪ An ability to take initiative and lead other;
▪ An ability to use software where relevant to the subject.</td></tr>
<tr><td>11.</td><td colspan="6">Teaching-learning and assessment strategy

A variety of learning strategies are used throughout the course, including the following
• Classroom Lesson; Lecturer and power point presentation
• Tutorial session
• Student- lecturer Discussion
• Collaborative and co-operative learn;</td></tr>
</table>

	• Independent study. **Assessment:** **Course works** **40%** Assignment 5% Tutorial 5% Quizzes 5% Laboratory works 10% Test 15% **Final Examination** **60%** **Total** **100%**
12.	**Synopsis:** This course is very important course in the field of electronics engineering. The objective of course is to provide students with advanced knowledge in digital design techniques and methodologies.
13.	**Mode of Delivery:** Lectures, Tutorials, Laboratory works

14.	**Assessment Methods and Types:** **Performance Criteria :**						
	CLO-PLO	**Assessment Tool**	**1**	**2**	**3**	**4**	**5**
	Marks		**0-39**	**40-49**	**50-59**	**60-74**	**75-100**
	Grade		**(F)**	**(D,D+)**	**(C-,C,C+)**	**(B-,B,B+)**	**(A-,A,A+)**
	CLO1: To introduce the IC design techniques;	**Assignment** **Tutorials** **Lab works** **Test** **Quizzes** **Examination**	**Fail To:** - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Poor To**: - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Satisfactory To**: - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Good To**: - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Excellent To:** - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test
	CLO2: To use engineering principles in hardware and software aspects of digital design;	**Assignment** **Tutorials** **Lab works** **Test** **Quizzes** **Examination**	**Fail To:** - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Poor To**: - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Satisfactory To**: - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Good To:** - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Excellent To:** - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test
	CLO3: To design, test and analyze the VLSI digital system's on FPGA platform;	**Assignment** **Tutorials** **Lab works** **Test** **Quizzes** **Examination**	**Fail To:** - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Poor To**: - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Satisfactory To**: - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Good To**: - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Excellent To:** - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test

15. **Mapping of the Programme Objectives to the Programme Learning Outcomes**

Programme Learning Outcomes (PLO) / Programme Objectives (PO)	**PLO1:** Ability to acquire and apply knowledge of science and engineering fundamentals.	**PLO2:** Acquired in-depth technical competence in electronics engineering discipline.	**PLO3:** Ability to undertake problem identification, formulation and solution;	**PLO4:** Ability to utilise systems approach to design and evaluate operational performance.	**PLO5:** Understanding of the principles of design for sustainable development;	**PLO6:** Understanding of professional and ethical responsibilities and commitment to them.	**PLO7:** Ability to communicate effectively, not only with engineers but also with the community at large.	**PLO8:** Ability to function effectively as an individual and in a group with the capacity to be a leader or manager;	**PLO9:** Understanding of the social, cultural, global and environmental responsibilities of a professional engineer	**PLO10:** Recognising the need to undertake lifelong learning, and possessing/acquiring the capacity to do so	**PLO11:** Ability become entrepreneur
PEO1: To produce graduates with excellent knowledge and competency in Electrical and Electronic Engineering;	✓		✓		✓						
PEO2: To produce graduates with professional, generic attributes to meet the present and future global demands.											
PEO3: To produce graduates with Islamic humanistic values and reinvention skills to meet the requirement of a dynamic environment. These skills include Civil Intelligence, Moral Intelligence, Self-Reliance and Communication Skills**.**											

16. **Mapping of the course Learning Outcome to the Programme Outcome**

Programme Learning Outcomes (PLO) / Course Learning Outcome (CLO)	**PLO1:** Ability to acquire and apply knowledge of science and engineering fundamentals.	**PLO2:** Acquired in-depth technical competence in electronics engineering discipline.	**PLO3:** Ability to undertake problem identification, formulation and solution;	**PLO4:** Ability to utilise systems approach to design and evaluate operational performance.	**PLO5:** Understanding of the principles of design for sustainable development;	**PLO6:** Understanding of professional and ethical responsibilities and commitment to them.	**PLO7:** Ability to communicate effectively, not only with engineers but also with the community at large.	**PLO8:** Ability to function effectively as an individual and in a group with the capacity to be a leader or manager;	**PLO9:** Understanding of the social, cultural, global and environmental responsibilities of a professional engineer	**PLO10:** Recognising the need to undertake lifelong learning, and possessing/acquiring the capacity to do so	**PLO11:** Ability become entrepreneur
CLO1: To introduce the IC design techniques;	✓		✓		✓						
CLO2 To use engineering principles in hardware and software aspects of digital design;	✓		✓		✓						
CLO3: To design, test and analyze the VLSI digital system's on FPGA platform;	✓		✓		✓						

17.	Content outline of the course/module and the SLT per topic						
	Details		**SLT(Hour)**				
			L	**T**	**P**	**IS**	**Total**
	Topic 1	**Introduction** Introduction to Digital VLSI Systems Design • Evolution of VLSI Systems. • Applications of VLSI Systems. • Processor based Systems. • Embedded Systems. • FPGA based Systems. • Digital System Design using FPGAs. • Reconfigurable Systems using FPGA. • Numbering Systems. • Twos Complement Addition/Subtraction. • Codes. • Boolean Algebra. • Boolean Functions using Minterms and Maxterms. • Logic Gates. • The Karnaugh MAP Method of Optimization of Logic Circuits. • Combination Circuits. • Arithmetic Logic Unit. • Programmable Logic Devices. • Sequential Circuits. • Random Access Memory (RAM). • Clock Parameters and Skew. • Setup, Hold and Propagation Delay Times in a Register. • Digital System Design using SSI/MSI Components. • Algorithmic State Machine. Digital System Design Using ASM Chart and PAL.	12	2	-	15	**29**
	Topic 2	**Design of Combinational and Sequential Circuits using Verilog.** • Introduction to Hardware Design Language. • Design of Combinational Circuits. • Verilog Modeling of Sequential Circuits. • Coding Organization**.** **Writing a Test Bench for the Design.** • Modeling a Test Bench. • Test Bench for Combinational Circuits. • Test Bench for Sequential Circuits.	9	2	-	12	**23**
	Topic 3	**Synthesis of Designs – Synplify Tool.** • Synthesis. • Analysis of Design Examples • Viewing Verilog Code as RTL Schematic Circuit Diagrams. • Optimization of design.	6	1	-	10	**17**

	Topic 4	**Place and Route and Back annotation** • Design Tool. • Place and Route Tool Place and Route and Back Annotation	3	-	-	8	**11**
	Topic 5	**Design of Memories.** • On-chip Dual Address ROM Design. • Single Address ROM Design. • On-Chip Dual RAM Design. • External Memory Controller Design**.**	6	1	-	10	**17**
	Topic 6	**Arithmetic Circuit Designs.** • Digital Pipelining. • Partitioning of a Design. • Signed Adder Design. Multiplier Design.	6	1	-	10	**17**
	Practical	**1.** Design and Simulation of Application Specific Control Unit**.** **2.** Design and Simulation of Datapath Unit. Students are required to design and simulate a digital system consisting of a control unit (Lab 1) and datapath unit (Lab 2). The digital system is chosen from a list of applications given by the instructor, or student-chosen topics that has obtained prior instructor's approval.	-	-	6	-	**6**
	Total SLT (Hour)		**42**	**7**	**6**	**65**	**120**
18.	**Main references supporting the course** 1. Ramachandran, Seetharaman, Digital VLSI Systems Design A Design Manual for Implementation of Projects on FPGAs and ASICs Using Verilog, Springer 2007.						
	Additional references supporting the course 1. John F. Wakerly, "Digital Design: Principles and Practices", 5th Ed, Prentice Hall, 2007.						
19.	**Other additional information** All materials will be available to the students in the library.						