<table>
<tr><td>1.</td><td colspan="5">Name of Course</td><td>Fabrication Technology</td></tr>
<tr><td>2.</td><td colspan="5">Course Code</td><td>JFAB2053</td></tr>
<tr><td></td><td colspan="6">JFAB = the first alphabet identify the faculty within which the subject is offered., JFAB = the remaining three alphabet identify the course that offers the subject, 2053= the first digit identify level of study; in this case undergraduate level, 2053= the second and third digits identify subject identity and 2053= the fourth digit identify credit value or credit hours</td></tr>
<tr><td>3.</td><td colspan="5">Name(s) of academic staff</td><td>To be Assigned</td></tr>
<tr><td>4.</td><td colspan="5">Rationale for the inclusion of the course/module in the programme</td><td>Knowledge of basic fabrication technology materials is essential in electronics engineering. Moreover, acquiring knowledge in fabrication enable engineer to design and fabricate semiconductor devices.</td></tr>
<tr><td>5.</td><td colspan="5">Semester and Year offered</td><td>Year 3, semester 1</td></tr>
<tr><td rowspan="3">6.</td><td colspan="2" rowspan="2">Total Student Learning Time (SLT)</td><td colspan="4">Face to Face</td><td rowspan="2">Total Guided and Independent Learning</td></tr>
<tr><td rowspan="2">L = Lecture T = Tutorial
P = Practical
IS = Independent Study</td><td>L</td><td>T</td><td>P</td><td>IS</td></tr>
<tr><td>42</td><td>7</td><td>6</td><td>65</td><td>Total Guided and Independent Learning = 120</td></tr>
<tr><td>7.</td><td colspan="5">Credit Value</td><td>3.0</td></tr>
<tr><td></td><td colspan="6">Lecture: 3 hours per week x 14 weeks
Tutorial: 1 hour per week x 7 weeks
Practical: 2 hours x 3 weeks</td></tr>
<tr><td>8.</td><td colspan="5">Prerequisite (if any)</td><td>JDLD1033: Digital Logic Design</td></tr>
<tr><td>9.</td><td colspan="6">Course Objectives
1. To introduce the fabrication technology;
2. To equip the students with the knowledge of the semiconductor materials and its properties.

Course Learning Outcomes (CLO)
At the end of the semester students should be able to:

CLO1: To demonstrate the fundamentals of semiconductor fabrication technology, from crystal growth to IC assembly;
CLO2: To understand the stages of IC manufacturing including wafer substrate preparation, wafer fabrication, wafer sorting and wafer assembly;
CLO3: To comprehend the concepts of Photolithography and Etching in monolithic IC fabrication.</td></tr>
<tr><td>10.</td><td colspan="6">Transferable Skills:
This course is expected the development of the following transferable skills:
▪ An ability to manage time and task
▪ An ability to learn both independently and co—operatively;
▪ An ability to take responsibility and carry out laboratory test;
▪ An ability to take initiative and lead other;
▪ An ability to use software where relevant to the subject.</td></tr>
<tr><td>11.</td><td colspan="6">Teaching-learning and assessment strategy

A variety of learning strategies are used throughout the course, including the following
• Classroom Lesson; Lecturer and power point presentation
• Tutorial session
• Student- lecturer Discussion</td></tr>
</table>

- Collaborative and co-operative learn;
- Independent study.

Assessment:

Course works		**40%**
Assignment	5%	
Tutorial	5%	
Quizzes	5%	
Laboratory works	10%	
Test	15%	
Final Examination		**60%**
Total		**100%**

12. **Synopsis:**
This course is very important course in the field of electronic engineering. The objective of course is to introduce students to the fundamentals of VLSI Fabrication technology.

13. **Mode of Delivery:**
Lectures,
Tutorials,
Laboratory works

14. **Assessment Methods and Types:**
Performance Criteria :

CLO-PLO	Assessment Tool	1	2	3	4	5
Marks		**0-39**	**40-49**	**50-59**	**60-74**	**75-100**
Grade		**(F)**	**(D,D+)**	**(C-,C,C+)**	**(B-,B,B+)**	**(A-,A,A+)**
CLO1: To demonstrate the fundamentals of semiconductor fabrication technology, from crystal growth to IC assembly;	**Assignment** **Tutorials** **Lab works** **Quizzes** **Test** **Examination**	**Fail To:** - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Poor To**: - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Satisfactory To**: - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Good To**: - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Excellent To:** - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test
CLO2: To understand the stages of IC manufacturing including wafer substrate preparation, wafer fabrication, wafer sorting and wafer assembly;	**Assignment** **Tutorials** **Lab works** **Quizzes** **Test** **Examination**	**Fail To:** - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Poor To**: - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Satisfactory To**: - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Good To:** - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Excellent To:** - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test
CLO3: To comprehend the concepts of Photolithography and Etching in monolithic IC fabrication;	**Assignment** **Tutorials** **Lab works** **Quizzes** **Test** **Examination**	**Fail To:** - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Poor To**: - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Satisfactory To**: - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Good To**: - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Excellent To:** - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test

15. **Mapping of the Programme Objectives to the Programme Learning Outcomes**

Programme Learning Outcomes (PLO) / Programme Objectives (PO)	**PLO1:** Ability to acquire and apply knowledge of science and engineering fundamentals.	**PLO2:** Acquired in-depth technical competence in electrical and electronics engineering discipline.	**PLO3:** Ability to undertake problem identification, formulation and solution;	**PLO4:** Ability to utilise systems approach to design and evaluate operational performance.	**PLO5:** Understanding of the principles of design for sustainable development;	**PLO6:** Understanding of professional and ethical responsibilities and commitment to them.	**PLO7:** Ability to communicate effectively, not only with engineers but also with the community at large.	**PLO8:** Ability to function effectively as an individual and in a group with the capacity to be a leader or manager;	**PLO9:** Understanding of the social, cultural, global and environmental responsibilities of a professional engineer	**PLO10:** Recognising the need to undertake lifelong learning, and possessing/acquiring the capacity to do so	**PLO11:** Ability become entrepreneur
PEO1: To produce graduates with excellent knowledge and competency in Electrical and Electronic Engineering;	✓	✓	✓	✓							
PEO2: To produce graduates with professional, generic attributes to meet the present and future global demands.	✓	✓	✓	✓							
PEO3: To produce graduates with Islamic humanistic values and reinvention skills to meet the requirement of a dynamic environment. These skills include Civil Intelligence, Moral Intelligence, Self-Reliance and Communication Skills**.**	✓	✓	✓	✓							

16. **Mapping of the course Learning Outcome to the Programme Outcome**

Programme Learning Outcomes (PLO) / Course Learning Outcome (CLO)	**PLO1:** Ability to acquire and apply knowledge of science and engineering fundamentals.	**PLO2:** Acquired in-depth technical competence in electrical and electronics engineering discipline.	**PLO3:** Ability to undertake problem identification, formulation and solution;	**PLO4:** Ability to utilise systems approach to design and evaluate operational performance.	**PLO5:** Understanding of the principles of design for sustainable development;	**PLO6:** Understanding of professional and ethical responsibilities and commitment to them.	**PLO7:** Ability to communicate effectively, not only with engineers but also with the community at large.	**PLO8:** Ability to function effectively as an individual and in a group with the capacity to be a leader or manager;	**PLO9:** Understanding of the social, cultural, global and environmental responsibilities of a professional engineer	**PLO10:** Recognising the need to undertake lifelong learning, and possessing/acquiring the capacity to do so	**PLO11:** Ability become entrepreneur
CLO1: To demonstrate the fundamentals of semiconductor fabrication technology, from crystal growth to IC assembly.	✓	✓	✓	✓							
CLO2: To understand the stages of IC manufacturing including wafer substrate preparation, wafer fabrication, wafer sorting and wafer assembly;	✓	✓	✓	✓							
CLO3: To comprehend the concepts of Photolithography and Etching in monolithic IC fabrication;	✓	✓	✓	✓							

17. **Content outline of the course/module and the SLT per topic**

Details		SLT (Hour)				
		L	**T**	**P**	**IS**	**Total**
Topic 1	**Introduction** • Crystal Growth and Wafer Preparation • Photolithography and Etching • Film Deposition and Oxidation • Diffusion and Ion Implantation • Interconnections and Contacts • Packaging and Yield	3	-	-	6	**9**
Topic2	**Crystal Growth and Wafer Preparation** • Electronic-Grade Silicon, • Czochralski Crystal Growing, • Silicon Shaping, • Processing Considerations	3	-	-	6	**9**
Topic 3	**Photolithography and Etching** • Wafer Cleaning, • Barrier Layer Formation, • Photoresist Application, • Soft Baking, Mask Alignment, • Photoresist Exposure and Development, • Hard Baking, • Wet Chemical Etching, • Dry Etching, • Photoresist Removal, • Photomask Fabrication	9	2	-	13	**24**
Topic 4	**Film Deposition and Oxidation** • Evaporation Techniques, • Sputtering, • Chemical Vapor Deposition, • Epitaxy **Diffusion and Ion Implantation** • Diffusion Process, • Diffusion Coefficient, • Successive Diffusions, • Solid-Solubility Limits, • Junction Formation and Characterization, • Sheet Resistance, • Diffusion Systems, • Implantation Technology, • Selective Implantation, • Junction Depth, • Channeling, • Lattice Damage, Annealing	12	3	-	17	**32**

	Topic 5	**Interconnections and Contacts** • Ohmic Contact Formation, • Aluminum-Silicon Eutectic Behavior, • Aluminum Spiking and Junction Penetration, • Contact Resistance, • Electromigration, • Diffused Interconnections, • Polysilicon Interconnections, • Buried Contacts, Butted Contacts, • Silicides, • Multilayer Contacts, • Liftoff Process, • Multilevel Metallization	9	2	-	13	**24**
	Topic6	**Packaging and Yield** • Testing, • Die Separation, • Die Attachment, • Wire Bonding, • Packages, • Flip-Chip Process, • Tape-Automated-Bonding Process, • Yield, • Uniform and Nonuniform Defect Densities	6	-	-	10	**16**
	Practical	1. Simulation of Diffusion Processes 2. Simulation of a Complete Fabrication Process	-	-	6	-	**6**
	Total SLT (Hour)		**42**	**7**	**6**	**65**	**120**
18.	**Main references supporting the course** 1. Stephen A. Campbell, "Fabrication Engineering at the Micro- and Nanoscale", 4th ed., Oxford University Press, 2009.						
	Additional references supporting the course						
19.	**Other additional information** All materials will be available to the students in the library.						