<table>
<tr><td>1.</td><td colspan="5">Name of Course</td><td>CMOS Integrated Circuits</td></tr>
<tr><td>2.</td><td colspan="5">Course Code</td><td>JMOS4063</td></tr>
<tr><td></td><td colspan="6">JMOS= the first alphabet identify the faculty within which the subject is offered., JMOS= the remaining three alphabet identify the course that offers the subject, 4063 = the first digit identify level of study; in this case undergraduate level, 4063= the second and third digits identify subject identity and 4063 = the fourth digit identify credit value or credit hours</td></tr>
<tr><td>3.</td><td colspan="5">Name(s) of academic staff</td><td>To be Assigned</td></tr>
<tr><td>4.</td><td colspan="5">Rationale for the inclusion of the course/module in the programme</td><td>Knowledge of CMOS Integrated Circuits is essential in electronic engineering. Moreover, acquiring knowledge in CMOS Integrated Circuits enable engineer to design CMOS analog integrated circuits.</td></tr>
<tr><td>5.</td><td colspan="5">Semester and Year offered</td><td>Year 4, Semester 1</td></tr>
<tr><td rowspan="3">6.</td><td colspan="2">Total Student Learning Time (SLT)</td><td colspan="4">Face to Face</td><td>Total Guided and Independent Learning</td></tr>
<tr><td colspan="2" rowspan="2">L = Lecture T = Tutorial
P = Practical
IS= Independent Study</td><td>L</td><td>T</td><td>P</td><td>IS</td><td rowspan="2">Total Guided and Independent Learning = 120</td></tr>
<tr><td>42</td><td>7</td><td>6</td><td>65</td></tr>
<tr><td>7.</td><td colspan="5">Credit Value</td><td>3.0</td></tr>
<tr><td></td><td colspan="6">Lecture: 3 hours per week x 14 weeks
Tutorial: 1 hour per week x 14 weeks
Practical: 2 hours x 5 weeks</td></tr>
<tr><td>8.</td><td colspan="5">Prerequisite (if any)</td><td>JELT1023: Electronics II</td></tr>
<tr><td>9.</td><td colspan="6">Course Objectives
1. To introduce the CMOS Integrated Circuits;
2. To equip the students with the knowledge of analysis and design of CMOS analog integrated circuits..

Course Learning Outcomes (CLO)
At the end of the semester students should be able to:

CLO1: To describe the basic operation of MOSFETs;
CLO2: To analyze and design basic MOSFET amplifier configurations and current mirrors;
CLO3: To analyze and design single-ended MOSFET operational amplifiers.</td></tr>
<tr><td>10.</td><td colspan="6">Transferable Skills:
This course is expected the development of the following transferable skills:
▪ An ability to manage time and task
▪ An ability to learn both independently and co—operatively;
▪ An ability to take responsibility and carry out laboratory test;
▪ An ability to take initiative and lead other;
▪ An ability to use software where relevant to the subject.</td></tr>
<tr><td>11.</td><td colspan="6">Teaching-learning and assessment strategy

A variety of learning strategies are used throughout the course, including the following
• Classroom Lesson; Lecturer and power point presentation
• Tutorial session
• Student- lecturer Discussion
• Collaborative and co-operative learn;
• Independent Study.</td></tr>
</table>

	Assessment:		
	Course works		**40%**
	Assignment	5%	
	Tutorial	5%	
	Quizzes	5%	
	Laboratory works	10%	
	Test	15%	
	Final Examination		**60%**
	Total		**100%**
12.	**Synopsis:** This course is very important course in the field of electronic engineering. The objective of course is to introduce students to the analysis and design of CMOS analog integrated circuits.		
13.	**Mode of Delivery:** Lectures; Tutorials; Laboratory Works		

14. **Assessment Methods and Types:**
Performance Criteria :

CLO-PLO	**Assessment Tool**	**1**	**2**	**3**	**4**	**5**
Marks		**0-39**	**40-49**	**50-59**	**60-74**	**75-100**
Grade		**(F)**	**(D,D+)**	**(C-,C,C+)**	**(B-,B,B+)**	**(A-,A,A+)**
CLO1: To describe the basic operation of MOSFETs.	**Assignment** **Tutorials** **Quizzes** **Lab works** **Test** **Examination**	**Fail To:** - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Poor To**: - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Satisfactory To**: - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Good To**: - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Excellent To:** - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test
CLO2: To analyze and design basic MOSFET amplifier configurations and current mirrors;	**Assignment** **Tutorials** **Quizzes** **Lab works** **Test** **Examination**	**Fail To:** - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Poor To**: - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Satisfactory To**: - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Good To:** - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Excellent To:** - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test
CLO3: To analyze and design single-ended MOSFET operational amplifiers;	**Assignment** **Tutorials** **Quizzes** **Lab works** **Test** **Examination**	**Fail To:** - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Poor To**: - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Satisfactory To**: - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Good To**: - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test	**Excellent To:** - manage time and task - learn both independently and cooperatively - take responsibility and carry out laboratory test

15. **Mapping of the Programme Objectives to the Programme Learning Outcomes**

Programme Learning Outcomes (PLO) / Programme Objectives (PO)	**PLO1:** Ability to acquire and apply knowledge of science and engineering fundamentals.	**PLO2:** Acquired in-depth technical competence in electronic engineering discipline.	**PLO3:** Ability to undertake problem identification, formulation and solution;	**PLO4:** Ability to utilise systems approach to design and evaluate operational performance.	**PLO5:** Understanding of the principles of design for sustainable development;	**PLO6:** Understanding of professional and ethical responsibilities and commitment to them.	**PLO7:** Ability to communicate effectively, not only with engineers but also with the community at large.	**PLO8:** Ability to function effectively as an individual and in a group with the capacity to be a leader or manager;	**PLO9:** Understanding of the social, cultural, global and environmental responsibilities of a professional	**PLO10:** Recognising the need to undertake lifelong learning, and possessing/acquiring the capacity to do so	**PLO11**: Ability become entrepreneur
PEO1: To produce graduates with excellent knowledge and competency in Electrical and Electronic Engineering;	✓	✓	✓								
PEO2: To produce graduates with professional, generic attributes to meet the present and future global demands;											
PEO3: To produce graduates with Islamic humanistic values and reinvention skills to meet the requirement of a dynamic environment. These skills include Civil Intelligence, Moral Intelligence, Self-Reliance and Communication Skills.											

16. **Mapping of the course Learning Outcome to the Programme Outcome**

Programme Learning Outcomes (PLO) / Course Learning Outcome (CLO)	**PLO1:** Ability to acquire and apply knowledge of science and engineering fundamentals.	**PLO2:** Acquired in-depth technical competence in electronic engineering discipline.	**PLO3:** Ability to undertake problem identification, formulation and solution;	**PLO4:** Ability to utilise systems approach to design and evaluate operational performance.	**PLO5:** Understanding of the principles of design for sustainable development;	**PLO6:** Understanding of professional and ethical responsibilities and commitment to them.	**PLO7:** Ability to communicate effectively, not only with engineers but also with the community at large.	**PLO8:** Ability to function effectively as an individual and in a group with the capacity to be a leader or manager;	**PLO9:** Understanding of the social, cultural, global and environmental responsibilities of a professional engineer	**PLO10:** Recognising the need to undertake lifelong learning, and possessing/acquiring the capacity to do so	**PLO11**: Ability become entrepreneur
CLO1: To describe the basic operation of MOSFETs;	✓	✓	✓								
CLO2: To analyze and design basic MOSFET amplifier configurations and current mirrors;	✓	✓	✓								
CLO3: To analyze and design single-ended MOSFET operational amplifiers;	✓	✓	✓								

17.	**Content outline of the course/module and the SLT per topic**							
	Details		**SLT (Hour)**					
			L	**T**	**P**	**IS**	**Total**
	Topic 1	**Basic MOS Device Physics** • MOSFET as a Switch , • MOSFET Structure , • MOS Symbols MOS I/V Characteristics , • Threshold , • Derivation of I/V Characteristics , • Second-Order Effects MOS Device Models MOS Device Layout • MOS Device Capacitances , • MOS Small-Signal Model , • MOS SPICE models , • NMOS versus PMOS Devices , Long-Channel versus Short-Channel Devices **Single-Stage Amplifiers** • Common-Source Stage , • Common-Source Stage with Resistive Load , • CS Stage with Diode-Connected Load , • CS Stage with Current-Source Load , • CS Stage with Triode Load , • CS Stage with Source Degeneration , • Source Follower. • Common-Gate Stage, • Cascode Stage , • Folded Cascode • Choice of Device Models	9	2	-	13	**24**
	Topic 2	**Differential Amplifiers** • Single-Ended and Differential Operation, • Basic Differential Pair , • Qualitative Analysis , • Quantitative Analysis , • Common-Mode Response , • Differential Pair with MOS Loads. • Gilbert **Passive and Active Current Mirrors** • Basic Current Mirrors , • Cascode Current Mirrors , • Active Current Mirrors, • Large-Signal Analysis , • Small-Signal Analysis , Common-Mode Properties	9	2	-	12	**23**

	Topic 3	**Frequency Response of Amplifiers** • Miller Effect , • Association of Poles with Nodes , • Common-Source Stage, • Source Followers, Common-Gate Stage , • Cascode Stage **Noise** • Noise Spectrum , • Amplitude Distribution , • Correlated and Uncorrelated Sources, • Types of Noise, Thermal Noise . . . . Flicker Noise , • Representation of Noise in Circuits , • Noise in Single-Stage Amplifiers , • Common-Source Stage , • Common-Gate Stage, • Source Followers , Cascode	9	2	-	12	**23**
	Topic 4	**Feedback** • Properties of Feedback Circuits , • Types of Amplifiers. • Feedback Topologies, • Voltage-Voltage Feedback Current-Voltage Feedback, • Voltage-Current Feedback • Current-Current Feedback • Effect of Loading • Two-Port Network Models, • Loading in Voltage-Voltage, • Current-Voltage • Voltage-Current • Current-Current Feedback **Operational Amplifiers.** • Performance Parameters, • One-Stage Op Amps. . • Two-Stage Op Amps , • Gain Boosting, • Comparison, • Common-Mode Feedback • Input Range Limitations, • Slew Rate , • Power Supply Rejection, • Noise in Op Amps	9	1	-	12	**22**
	Topic 5	**Stability and Frequency Compensation** • Multipole Systems • Phase Margin • Frequency Compensation • Compensation of Two-Stage Op Amps • Slewing in Two-Stage Op Amps	3	-	-	8	**11**

	Topic 6	**Oscillators** • Ring Oscillators, • LC Oscillators , • Crossed-Coupled Oscillator, • Colpitts Oscillator, • One-Port Oscillators. • Voltage-Controlled Oscillators. • Tuning in Ring Oscillators, • Tuning in LC Oscillators , • Mathematical Model of VCOs.	3	-	-	8	**11**
	Practical	• VLSI CAD software Tutorial- a detailed tutorial that walk students through the procedures of using these tools for the analysis and design of integrated circuits. • Single-stage amplifiers - carry out a detail analysis of time and frequency-domain characteristics of common-source, common-gate, and common-drain MOSFET amplifiers. • Voltage-mode operational amplifiers - prototype, design, analyze, and simulate a three-stage differential-input single-ended output operational amplifier. • Current-mode operational amplifiers - prototype, design, analyze, and simulate a two-stage differential-input differential-output current amplifier. • Layout of voltage-mode operational amplifiers - develop the physical masks of the operational amplifier studied in Laboratory 3, extract the parasitic effects and perform post-Layout simulation of the designed operational amplifier.	-	-	6	-	**6**
	Total SLT (Hour)		**42**	**7**	**6**	**65**	**120**
18.	**Main references supporting the course** 1. Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill, 2006						
	Additional references supporting the course 1. Analysis and Design of Analog Integrated Circuits, Gray and Meyer, John Wiley & Sons, Fourth Edition, 2006						
19.	**Other additional information** All materials will be available to the students in the library.						